IN THE CLAIMS:

1-15. (Canceled)

16. (Currently Amended): A wafer for testing by a testing device, the wafer comprising:

a plurality of ~~similar~~ circuit ~~components~~ integrated circuits, wherein each ~~of~~ integrated circuit ~~components~~ includes testing circuitry;

a network of signal paths on the wafer, wherein the network of signal paths connects the plurality of integrated circuits to two or more connection points,

wherein in response to the testing device being connected to the connection points, the testing circuitry ~~tests~~ performs a test on the ~~circuit components~~ plurality of integrated circuits concurrently, and

wherein each integrated circuit includes at least one visible component having an appearance and wherein the at least one visible component permanently changes its appearance in response to failing the test.

17. (Currently Amended): The wafer of claim 16, wherein ~~each of the circuit~~ components ~~includes~~ a ~~visible~~ subcomponent ~~having an appearance and wherein the visible subcomponent changes its appearance in response to the testing circuitry finding the circuit component faulty~~ the at least one visible component includes at least one fuse.

18. (Currently Amended): The A wafer ~~of claim 16~~ for testing by a testing device, Uthe wafer ~~further~~ comprising:

a plurality of similar circuit components, wherein each of the circuit components includes testing circuitry, wherein in response to the testing device, the testing circuitry tests the circuit components concurrently; and

at least one interface point, wherein the testing device activates the testing circuitry through the at least one interface point.

19. (Original): The wafer of claim 18, further comprising:

a network of signal paths, wherein the network of signal paths connect the at least one interface point with the circuit components.

20. (Original): The wafer of claim 19, wherein the signal paths include a power supply signal path.

21. (Original): The wafer of claim 19, wherein the signal paths include a clock signal path.

22. (Original): The wafer of claim 19, wherein the signal paths include a control signal path.

23. (Original): The wafer of claim 19, wherein at least one of the signal paths is located on a scroll line.

24. (Original): The wafer of claim 19, wherein at least one of the signal paths is located on a die.

25-32. (Canceled)

33. (Currently Amended): A method of testing a circuit, comprising:

connecting a testing device to connection points on a wafer, wherein the wafer has fabricated thereon a plurality of integrated circuits and wherein each integrated circuit within the plurality of integrated circuits includes a testing circuit and a visible circuit component;

applying at least one signal to each testing ~~circuitry~~ circuit concurrently;

in response to a determination that ~~the~~ an integrated circuit from within the plurality of integrated circuits is defective, modifying a the visible circuit component in the defective integrated circuit to ha~~ve a differe~~nt permanently change appearance.

34. (Original): The method of claim 33, wherein modifying the visible circuit component includes destroying the visible circuit component.

35. (Currently Amended): The A method of ~~claim 33~~ testing a circuit, comprising:

applying at least one signal to testing circuitry;

in response to a determination that the circuit is defective, modifying a visible circuit component in the circuit to have a different appearance, wherein modifying the visible circuit component includes causing the visible circuit component to overheat.

36. (Currently Amended): The method of claim 33, wherein ~~the testing circuitry is built into the circuit~~ further comprising:

visually spotting, using a sorting device, any defective integrated circuits on the wafer.

37. (New): The method of claim 36, further comprising:

removing the defective integrated circuits from the wafer.

38. (New): The wafer of claim 17, wherein the at least one visible component includes at least one transistor.

39. (New): The wafer of claim 18, wherein the at least one transistor is a diode-connected transistor, the wafer further comprising:

a current mirror; and

a plurality of transistors,

wherein the current mirror receives a high current and passes an equal amount of current to each of the plurality of transistors, and

wherein the plurality of transistors, responsive to an input signal, pass current to the diode-connected transistor, causing the diode-connected transistor to burn up and leave a visible mark.

40. (New): The wafer of claim 16, wherein the network of signal paths includes a power supply signal path.

41. (New): The wafer of claim 16, wherein the network of signal paths includes a clock signal path.

42. (New): The wafer of claim 16, wherein the network of signal paths includes a control signal path.

43. (New): The wafer of claim 16, wherein the network of signal paths is located on a scroll line.